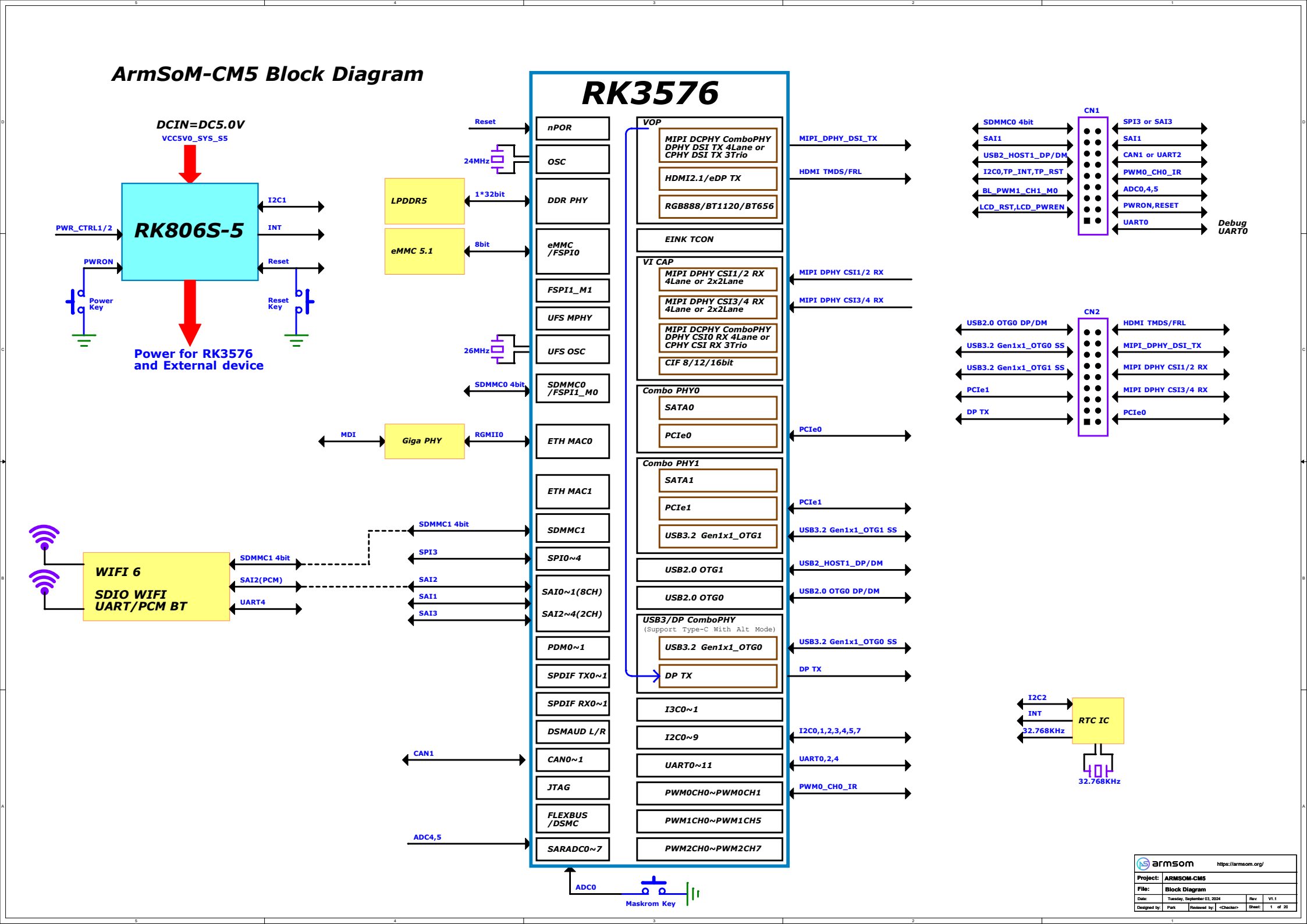
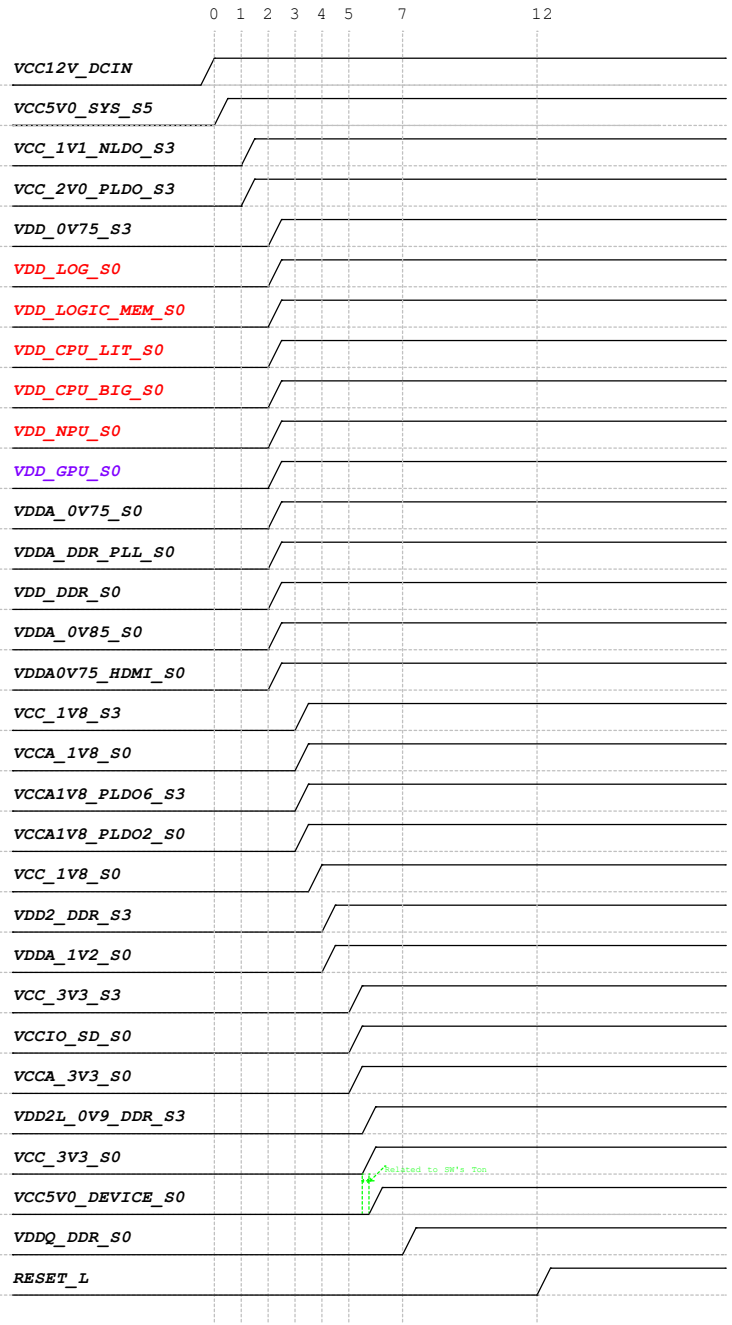
ArmSoM-CM5 Block Diagram



armsom	https://armsom.org/
Project:	ARMSOM-CM5
File:	Block Diagram
Date:	Tuesday, September 03, 2024
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	1 of 20

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

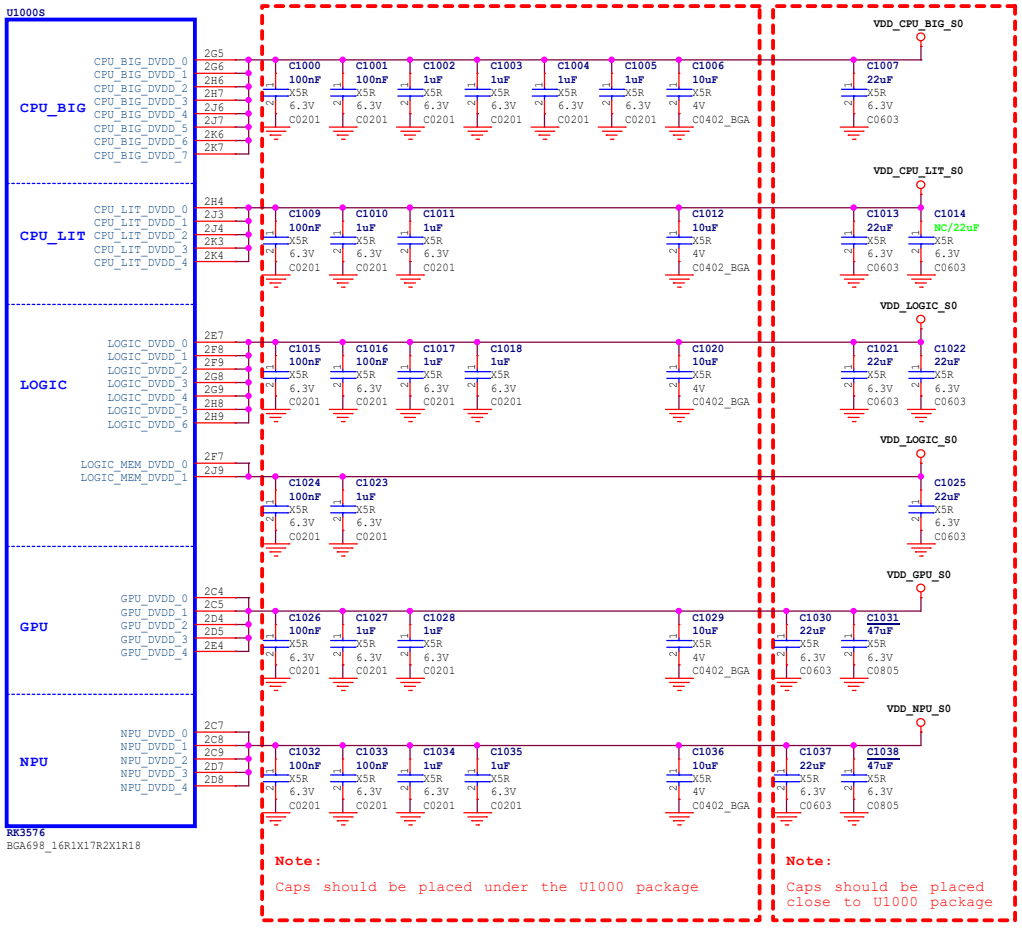
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

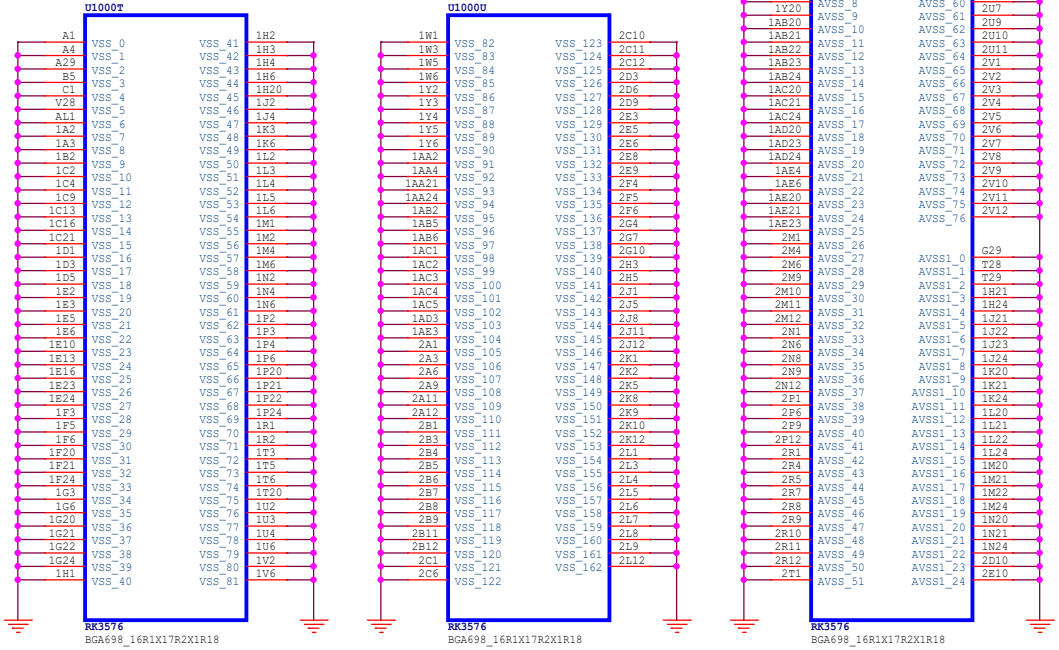
armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	Power Sequence and Map				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 20

RK3576_S (Power)

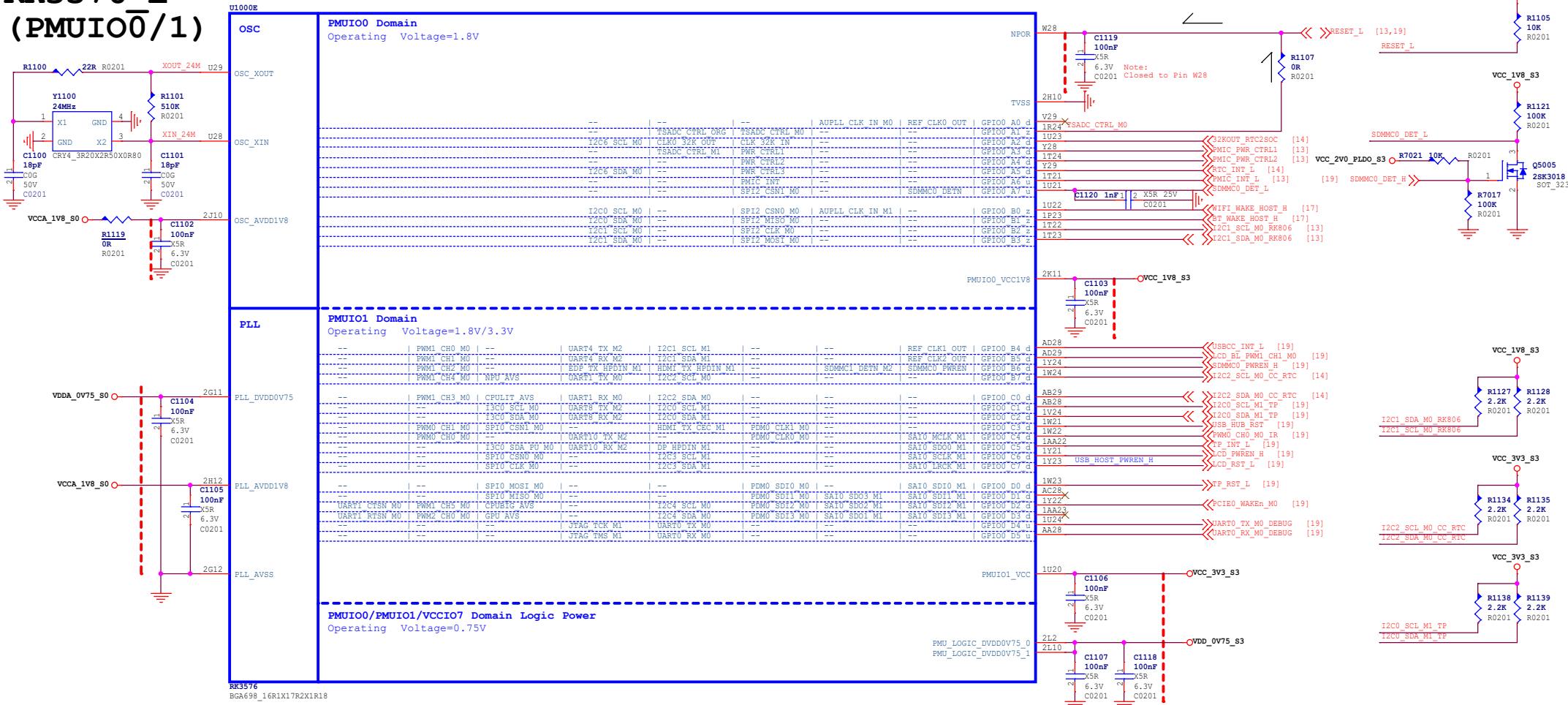


RK3576_T/U/V (GND)

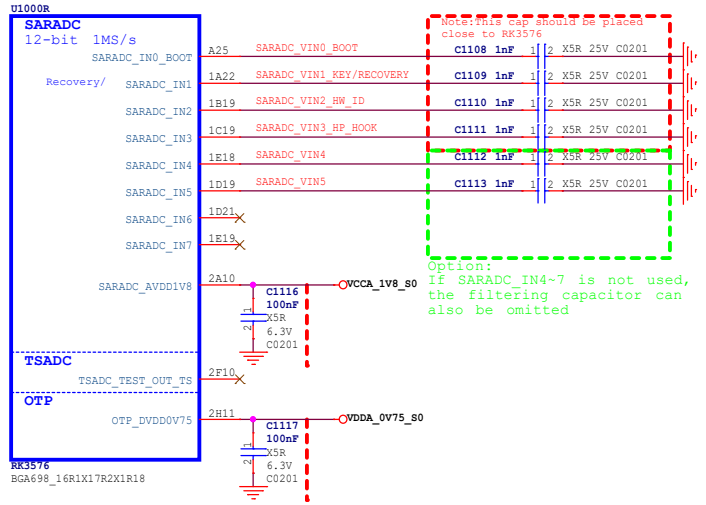


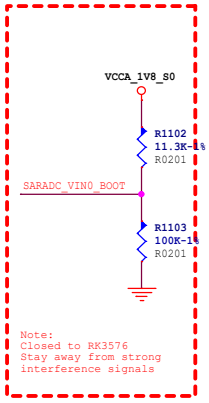
armsom	https://armsom.org/			
Project:	ARMSOM-CM5			
File:	RK3576-Power/GND			
Date:	Tuesday, September 03, 2024		Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	3 of 20

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)





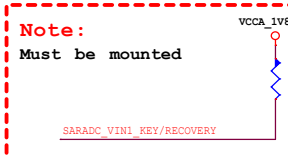
BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Must be mounted

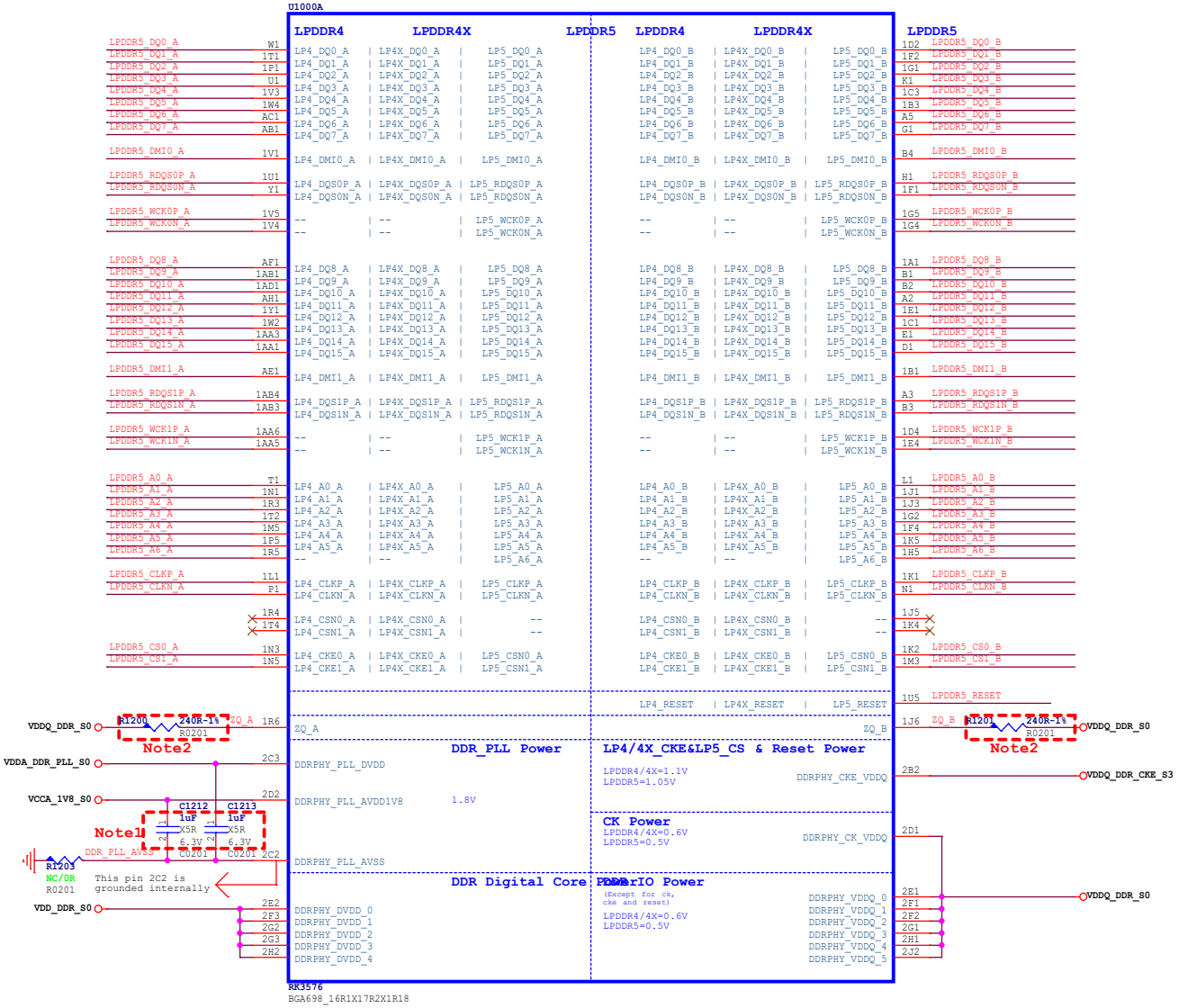


SARADC_VIN0_BOOT [19]
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_HW_ID
SARADC_VIN3_HP_HOOK
SARADC_VIN4 [19]
SARADC_VIN5 [19]

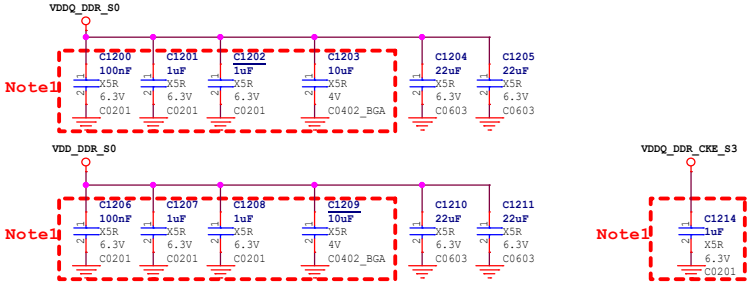
armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	RK3576-OSC/PLL/PMUIO/SARADC				
Date:	Monday, September 09, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	4 of 20

RK3576_A(DDRPHY)



DDR FILTER

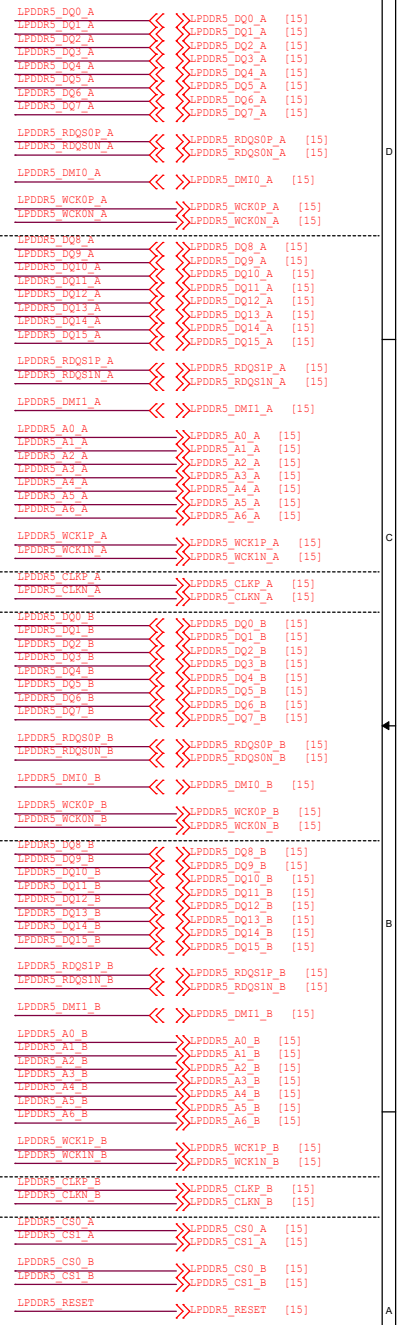


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

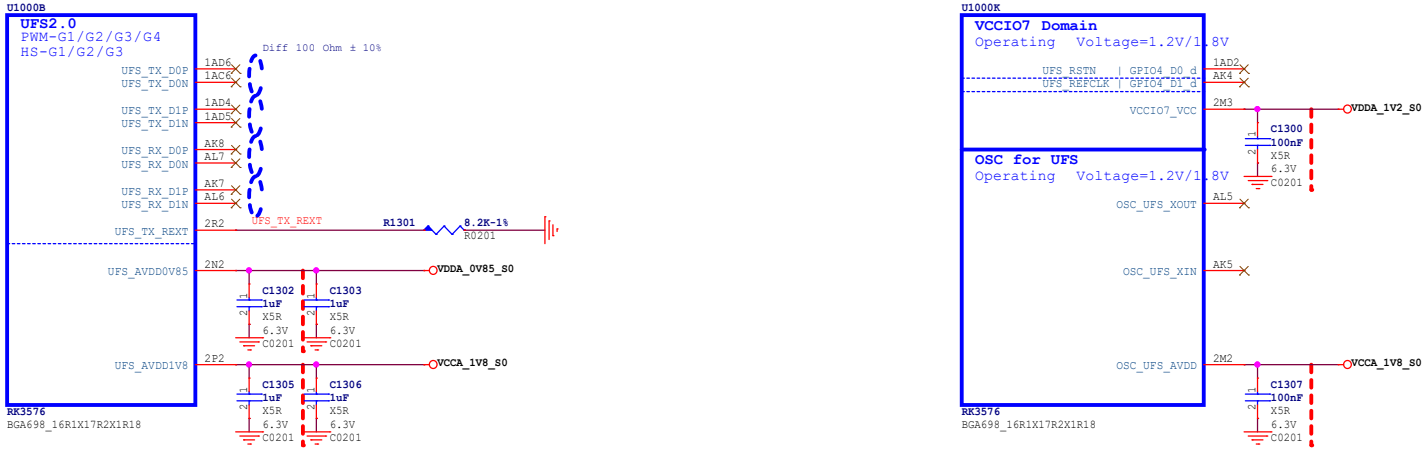
Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR5

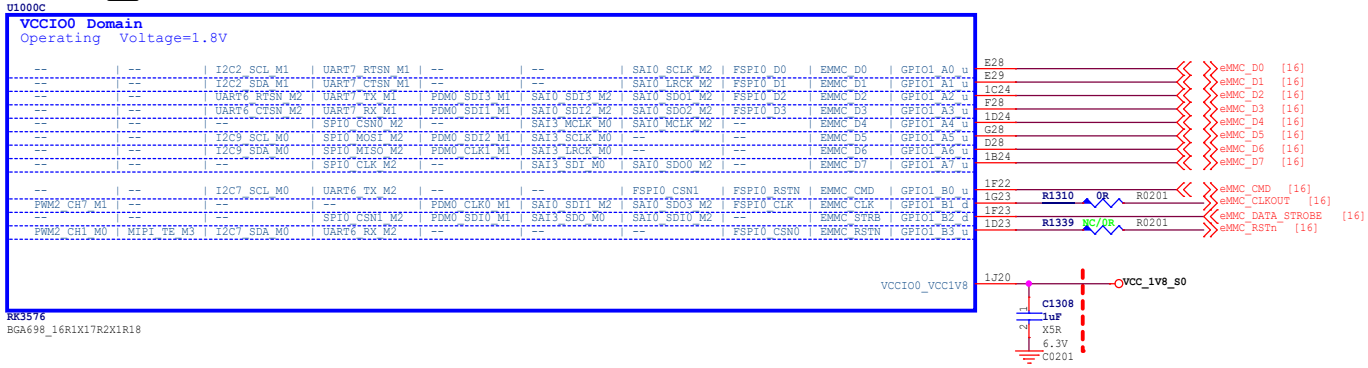


armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	RK3576-DDR PHY		
Date:	Tuesday, September 03, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 5 of 20

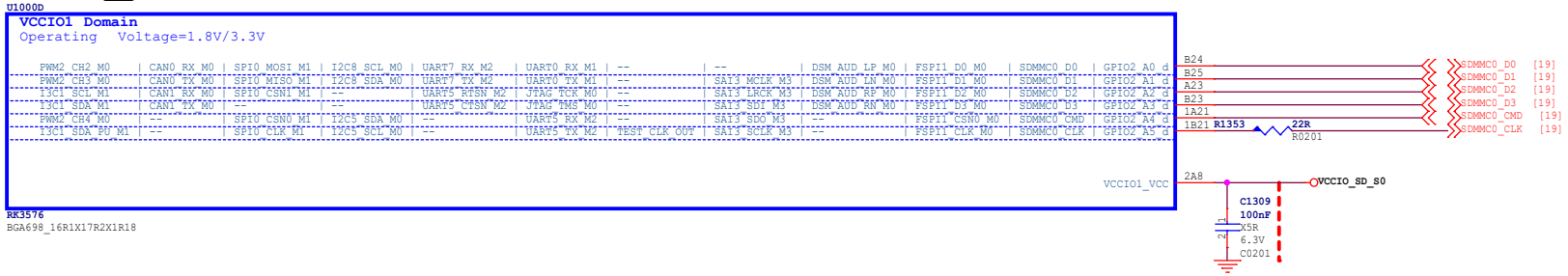
RK3576_B (UFS2.1)



RK3576_C (VCCIO0)



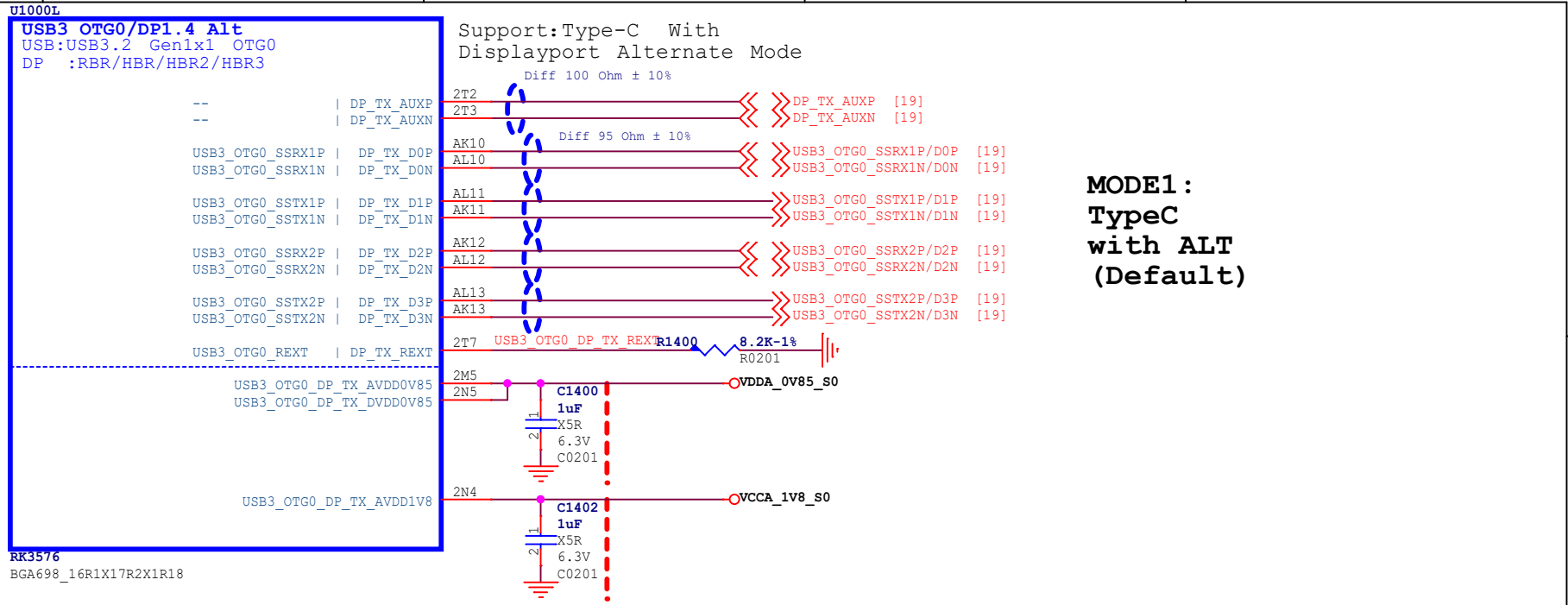
RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/			
Project:	ARMSOM-CM5			
File:	RK3576-eMMC/UFS/SD			
Date:	Tuesday, September 03, 2024		Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet:	6 of 20

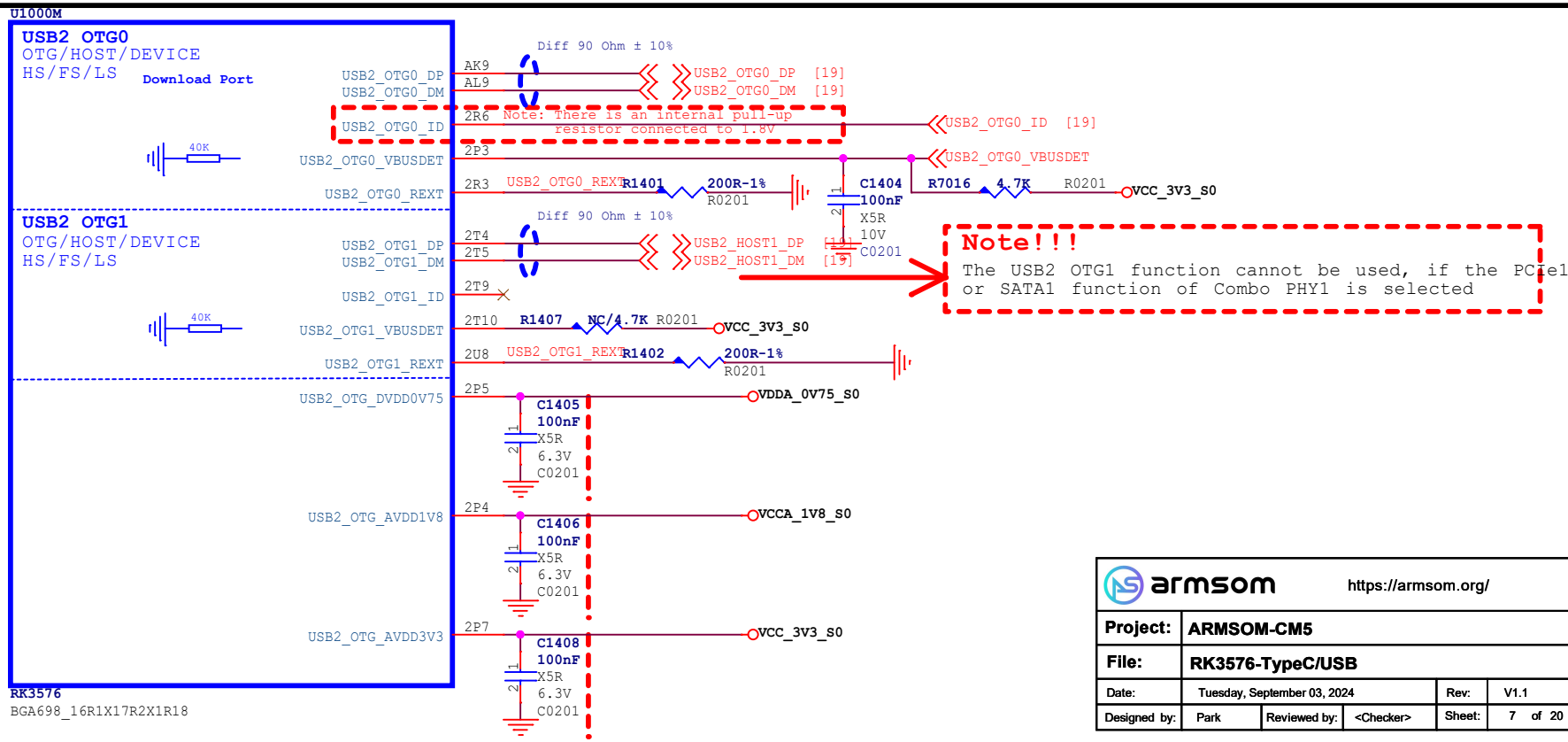
RK3576_L (USB3/DP)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

MODE1:
TypeC with ALT (Default)

RK3576_M (USB2)



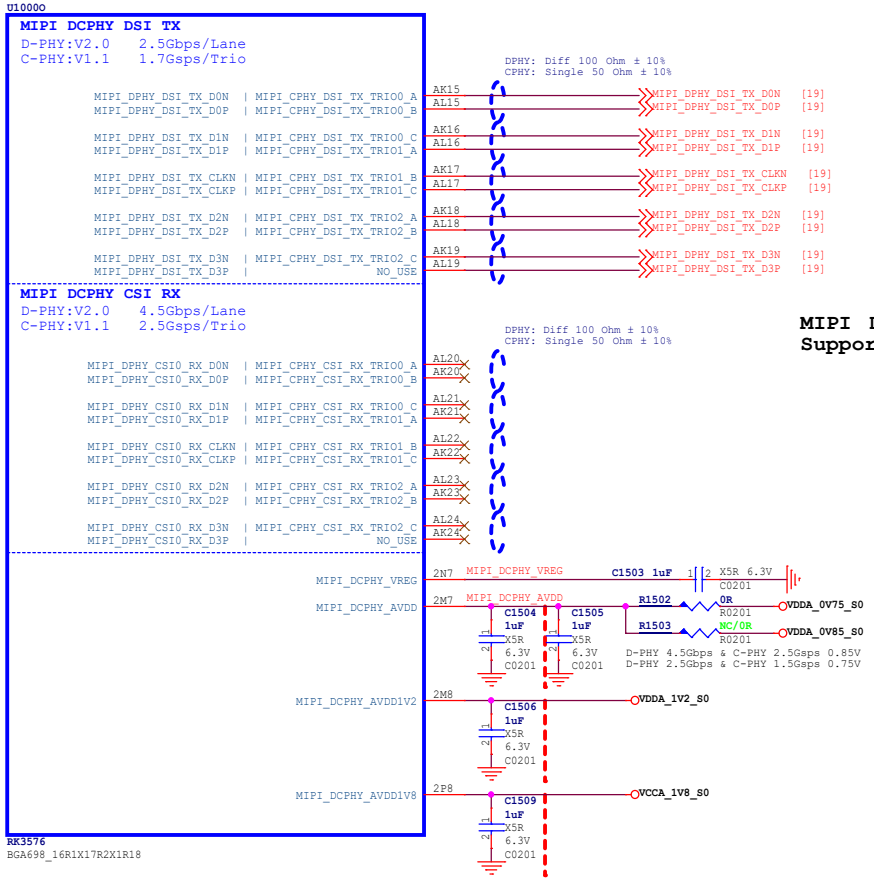
Note!!!
The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	RK3576-TypeC/USB				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 20

RK3576_O(MIPI DCPHY)

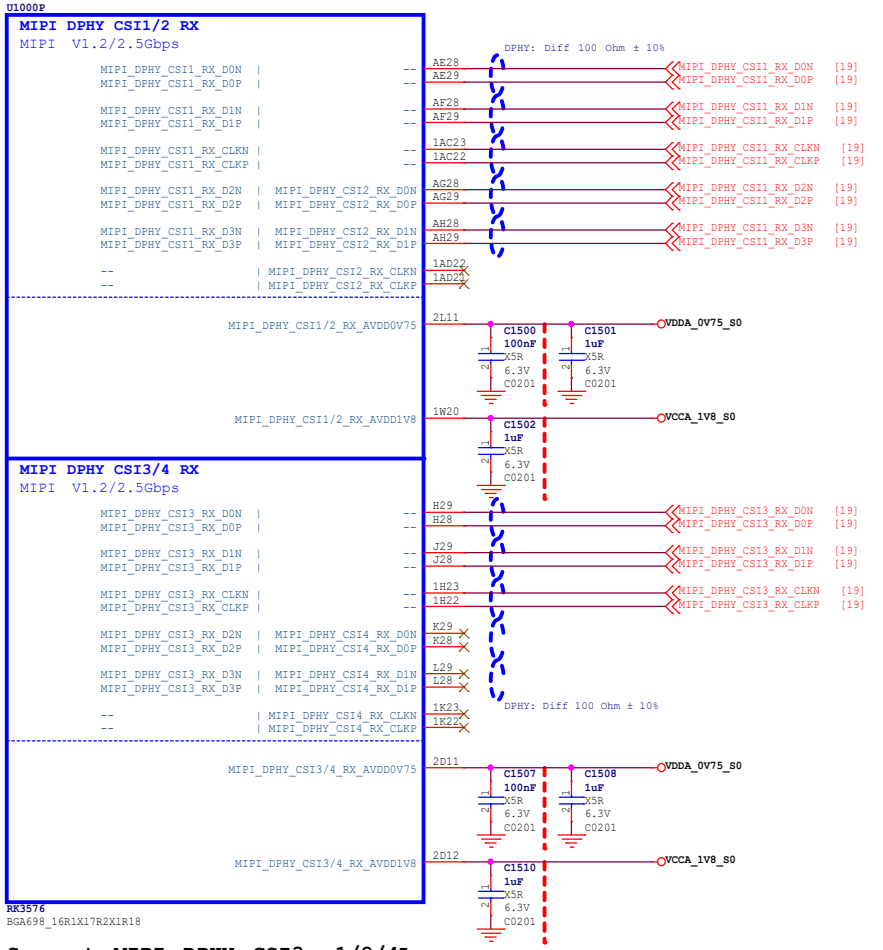


MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



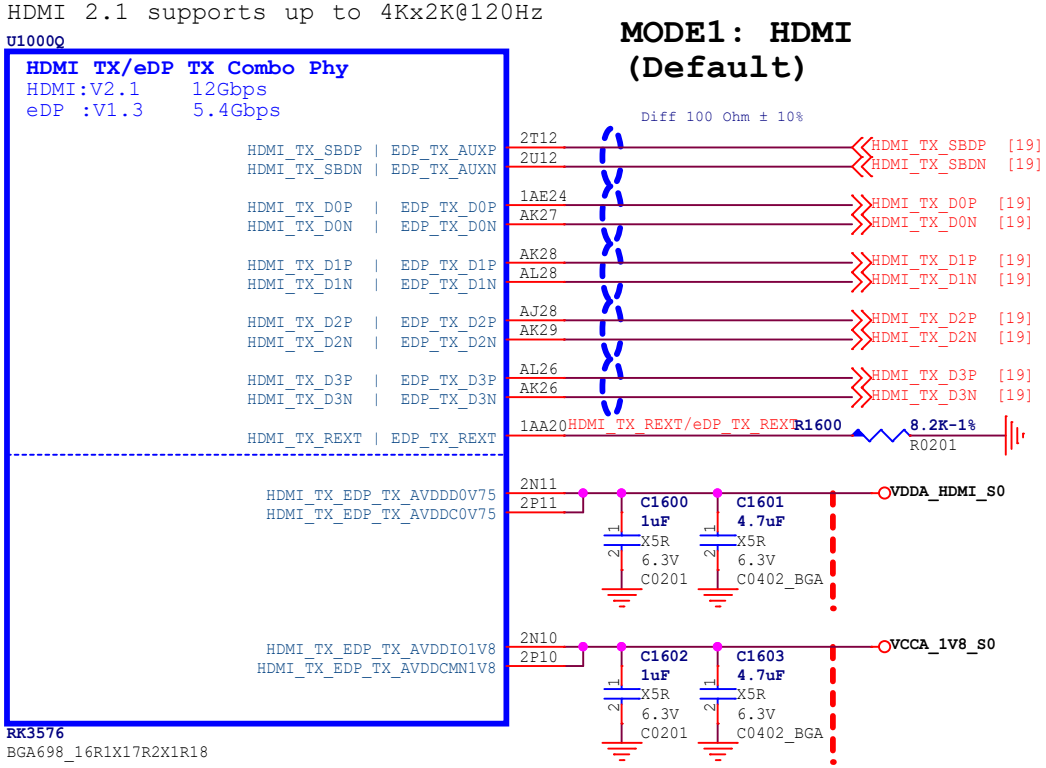
Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	RK3576-MIPI DSI/CSI				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 20

RK3576_Q(HDMI/eDP)

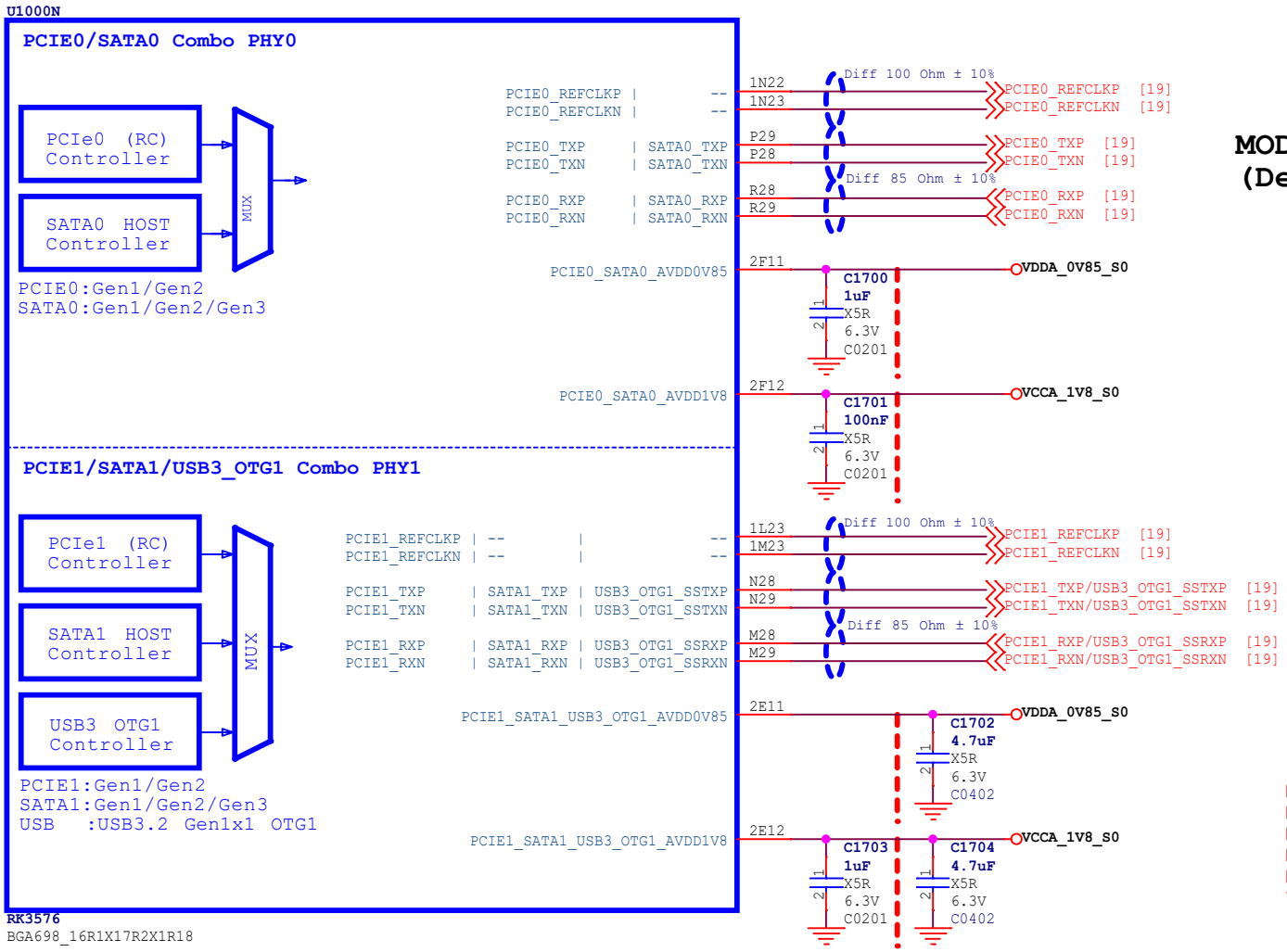
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	RK3576-HDMI/eDP				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 20

RK3576_N(PCIe/SATA/USB3)



MODE1: PCIe0 (Default)

Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 OTG1 function cannot be used

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	RK3576-PCIe/SATA/USB3				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	10 of 20

RK3576_F(VCCIO2)

U1000F

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d	1D6
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d	1C6
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d	1C5
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d	1B6
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d	1B5
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	GPIO4_A7_d	A7
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d	1A5
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d	B7
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d	B6
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d	1A6
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d	B8
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d	1A4

SAI1_MCLK_M0 [19]
SAI1_SCLK_M0 [19]
SAI1_LRCK_M0 [19]
SAI1_SDO0_M0 [19]
SAI1_SDO1_M0 [19]
SAI1_SDI0_M0 [19]
CAN1_RX/I2C3_SDA/UART_RX2 [19]
CAN1_TX/I2C3_SCL/UART_TX2 [19]

MODE1: HDMI RX Audio (Default)

VCCIO2_VCC 2A2 — C1800 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3576
BGA698_16R1X17R2X1R18

RK3576_G(VCCIO3)

U1000G

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d	A28
PWM1_CH1_M1	--	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d	B27
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d	1A23
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d	A27

PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d	B26
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d	1B22
PWM1_CH4_M1	--	SPI2_CSN1_M1	I2C8_SCL_M1	UART4_RTSN_M1	--	--	SPDIF_CSN1_M1	SPI1_RSTN_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_d	B29
--	--	SPI2_CSN0_M1	I2C8_SDA_M1	UART4_CTSN_M1	--	--	--	SPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d	1C23
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	SPI1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d	1B23
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	SPI1_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d	B28
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	SPI1_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d	A26
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	SPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d	1C22

--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d	C29
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d	1D22
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d	1A24
PWM1_CH4_M1	--	--	--	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d	C28
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d	1E21
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d	1E22

SDMMC1_D0_M0 [17]
SDMMC1_D1_M0 [17]
SDMMC1_D2_M0 [17]
SDMMC1_D3_M0 [17]
SDMMC1_CMD_M0 [17]
SDMMC1_CLK_M0 [17]
UART4_RTSN_M1 [17]
UART4_CTSN_M1 [17]
UART4_TX_M1 [17]
UART4_RX_M1 [17]
WIFI_REG_ON_H [17]
BT_REG_ON_H [17]
SAI2_SDO_M0 [17]
SAI2_SCLK_M0 [17]
SAI2_LRCK_M0 [17]
SAI2_SDI_M0 [17]
HOST_WAKE_BT_H [17]

VCCIO3_VCC 2B10 — C1801 100nF X5R 6.3V C0201 — VCCIO_WL

RK3576
BGA698_16R1X17R2X1R18

RK3576_J(VCCIO6)

U1000J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d	AK3
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d	AK2
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RF_M1	GPIO4_C2_d	AL2
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d	1AE2
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d	AL3
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d	AK1
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d	1AE1
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d	AJ1

HDMI_TX_CEC_M0 [19]
HDMI_TX_HPDIN_M0 [19]
HDMI_TX_SCL [19]
HDMI_TX_SDA [19]
TYPEC_DPTX_AUX_PUPDCTL1 [19]
TYPEC_DPTX_AUX_PUPDCTL2 [19]
HDMI_TX_ON_H [19]

C1803 1nF X5R 25V C0201

VCCIO6_VCC 2N3 — C1802 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3576
BGA698_16R1X17R2X1R18

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	RK3576-GPIO VCCIO2/3/6		
Date:	Monday, September 09, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 11 of 20

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d	B22
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d	B20
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d	B19
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d	1A18
--	--	PCIE0_CLKREQn_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d	1A17
--	--	PCIE1_CLKREQn_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d	1B16
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d	A19
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d	1C18
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d	A21
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d	B21
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d	A17
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d	1A15
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d	1D15
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_TXD2_M0	VI_CIF_D2	GPIO2_C3_d	A15
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDO_M0	SAI2_SDO_M1	--	ETH1_TXD3_M0	VI_CIF_D1	GPIO2_C4_d	1A13
PWM0_CH3_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCER_M0	VI_CIF_D0	GPIO2_C5_d	1C15
PWM1_CH4_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD1_M0	--	GPIO2_C6_d	1A14
PWM0_CH1_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD0_M0	--	GPIO2_C7_d	B15
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d	B16
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d	1A16
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d	B17
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d	B18
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d	1B13
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d	1B15
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d	1D18
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d	1E15
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d	1D16
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d	1B18
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d	1A20
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLK1	GPIO3_A3_d	1A19

RK3576

BGA698_16R1X17R2X1R18

VCCIO4_VCC — 2A7

C1900 NC/100nF X5R 6.3V C0201 — C1901 1uF X5R 6.3V C0201 — VCC_3V3_S0

B22 — PCIE0_PERSTn [19]
B20 — PCIE0_CLKREQn_M0 [19]
B19 — GMAC0_RSTn [18]
1A18 — MIPI_DPHY_CSI_CAM1_RST_H [19]
1A17 — OTG0_PWREN_H/UART7_TX/I2C8_SCL [19]
1B16 — HP_DET_L/UART7_RX/I2C8_SDA [19]
A19 — LED_GREEN_EN/UART4_TX/I2C6_SCL [19]
1C18 — LED_RED_EN/UART4_RX/I2C6_SDA [19]
A21 — PWM2_CH6_M2/SAI3_MCLK_M2 [19]
B21 — CAM_CLK2_OUT_M1_3V3 [19]
A17 — SPI3_CLK_M0/SAI3_SCLK_M2 [19]
1A15 — SPI3_MOSI_M0/SAI3_LRCK_M2 [19]
1D15 — SPI3_MISO_M0/SAI3_SDO_M2 [19]
A15 — SPI3_CSN0_M0/SAI3_SDI_M2 [19]
1A13
1C15
1A14
B15
B16
1A16
B17
B18
1B13
1B15
1D18
1E15
1D16
1B18
1A20
1A19

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d	1D13 GPIO3_A4
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d	A9
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d	1A7 GPIO3_A6
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d	B13
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d	B14
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d	1A11
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d	A13
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d	A11
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d	B10
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d	1A9
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d	B11
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d	1D12
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d	1E9
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO1_M1	ETH0_PPS_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d	1B10
PWM3_CH0_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d	B9
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d	1A8
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO0_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d	1D9
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO1_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d	1B9
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d	1D7
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d	1C7
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d	1C12
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d	1A12
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART12_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS1_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d	1A10
PWM2_CH5_M3	I3C1_SCL_M2	--	UART12_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d	B12
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d	1E12
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKF	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d	1D10
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d	1C10
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d	1E7
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d	1B12
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d	1B7

RK3576

BGA698_16R1X17R2X1R18

VCCIO5_VCC_0 / VCCIO5_VCC_1 — 2A4 / 2A5

C1902 NC/100nF X5R 6.3V C0201 — C1903 1uF X5R 6.3V C0201 — VCC_1V8_S0

1B12 — CAM1_CLK1_OUT_M0_1V8 [19]

VCC_1V8_S0 — R1926 2.2K R0201 — R1927 2.2K R0201 — I2C4_SDA_M3_MIPI_CAM2 / I2C4_SCL_M3_MIPI_CAM2

VCC_1V8_S0 — R1934 2.2K R0201 — R1935 2.2K R0201 — I2C5_SDA_M3_MIPI_CAM1 / I2C5_SCL_M3_MIPI_CAM1

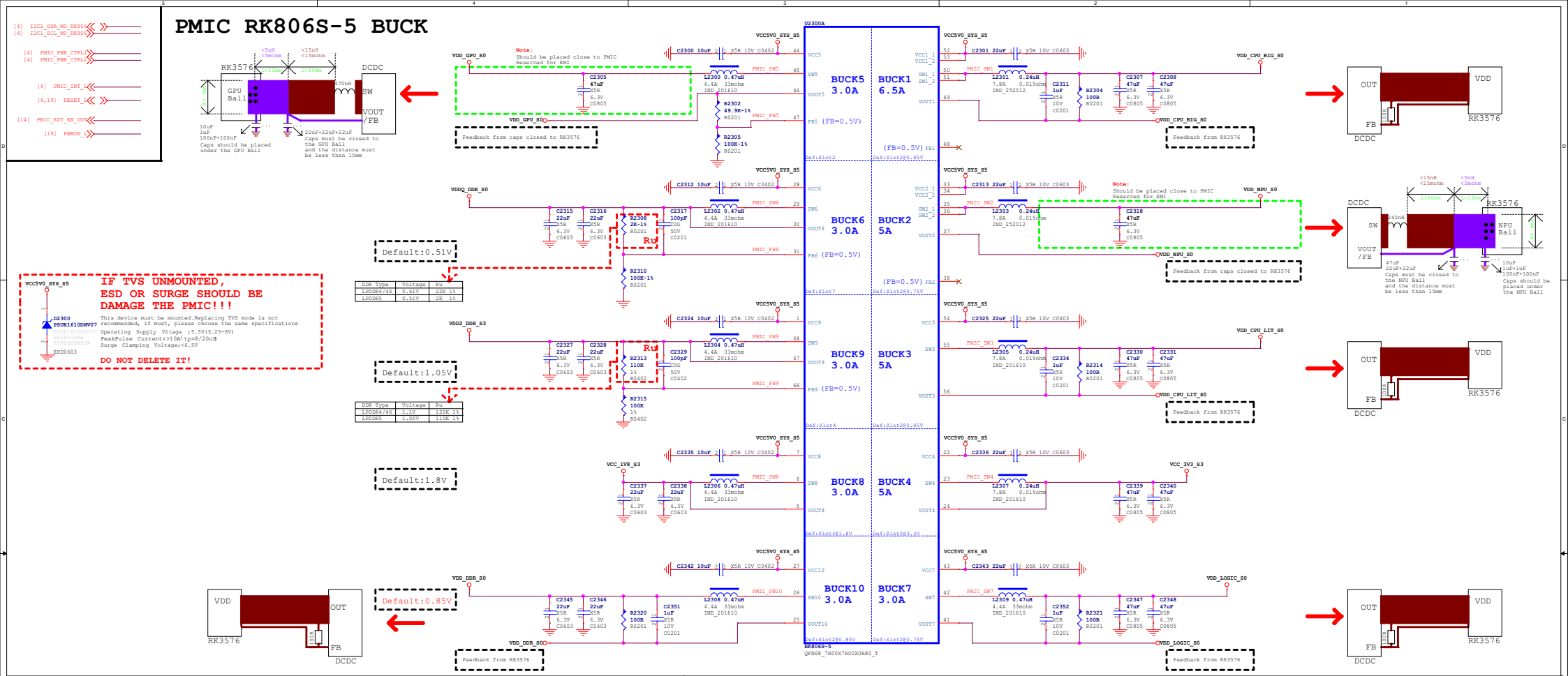
Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

B14 — MIPI_DPHY_CSI_CAM1_PDN_H [19]
1A11 — GMAC0_RXD1_M0 [18]
A13 — GMAC0_RXD0_M0 [18]
A11 — GMAC0_TXCTL_M0 [18]
B10 — GMAC0_TXD1_M0 [18]
1A9 — GMAC0_TXD0_M0 [18]
B11 — GMAC0_TXCLK_M0 [18]
1D12 — I2C4_SDA_M3_MIPI_CAM2 [19]
1E9 — I2C4_SCL_M3_MIPI_CAM2 [19]
1B10 — I2C5_SDA_M3_MIPI_CAM1 [19]
B9 — GMAC0_TXD3_M0 [18]
1A8 — GMAC0_TXD2_M0 [18]
1D9 — I2C5_SCL_M3_MIPI_CAM1 [19]
1C12 — GMAC0_RXCLK_M0 [18]
1A12 — GMAC0_RXD3_M0 [18]
1A10 — GMAC0_RXD2_M0 [18]
B12 — MIPI_DPHY_CSI_CAM2_PDN_H [19]
1E12 — MIPI_DPHY_CSI_CAM2_RST_H [19]
1D10
1C10
1E7

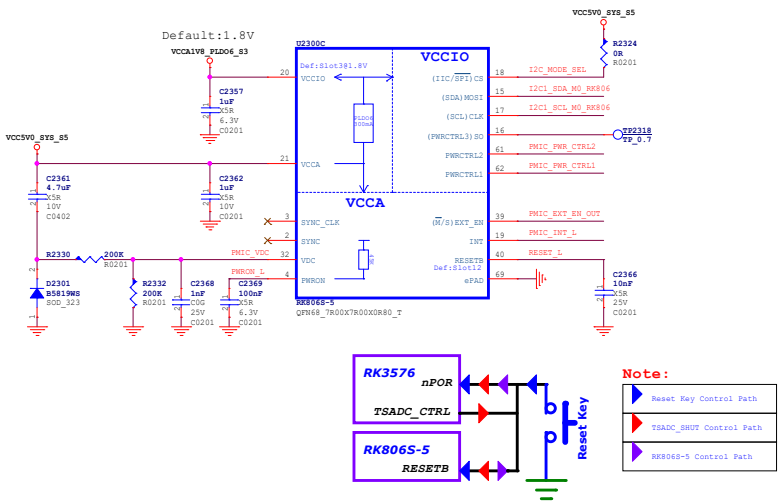
armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	RK3576-GPIO VCCIO4/5		
Date:	Monday, September 09, 2024	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 12 of 20

PMIC RK806S-5 BUCK

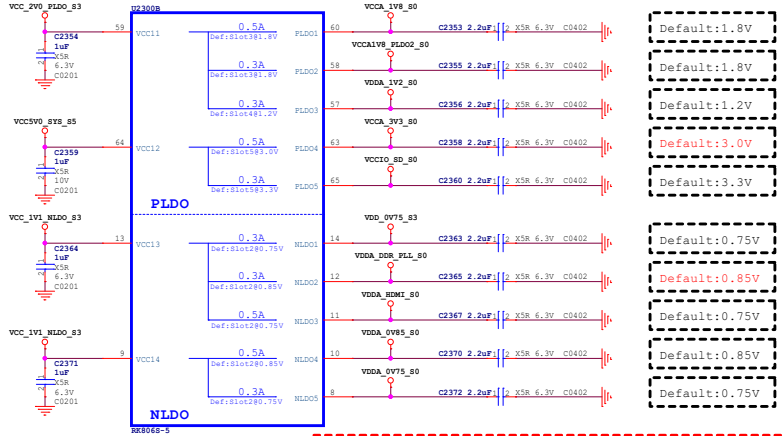


PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



PMIC RK806S-5 LDO

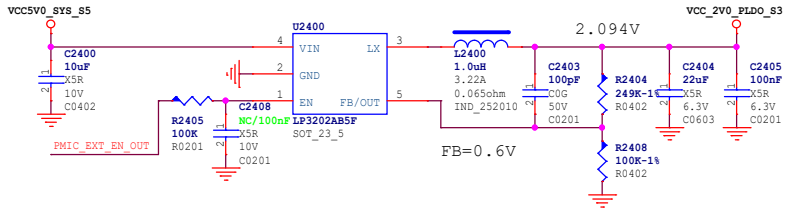


Note:
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

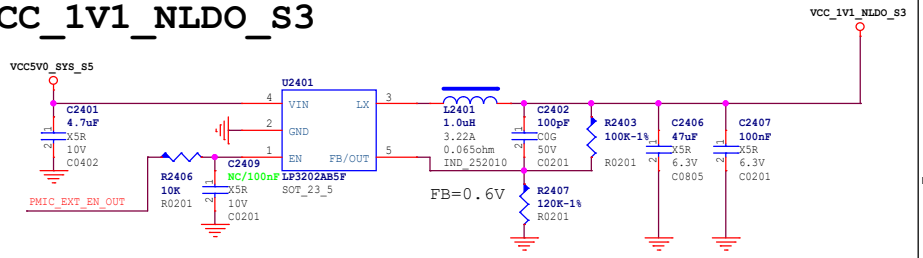
armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	Power-PMIC RK806S-5		
Date:	Monday, September 09, 2024	Rev.	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 13 of 20

[4] I2C2_SCL_M0_CC_RTC
[4] I2C2_SDA_M0_CC_RTC
[4] RTC_INT_L
[4] 32KOUT_RTC2SOC
[17] 32KOUT_RTC2WIFI
[13] PMIC_EXT_EN_OUT
[13,19] PWRON_L

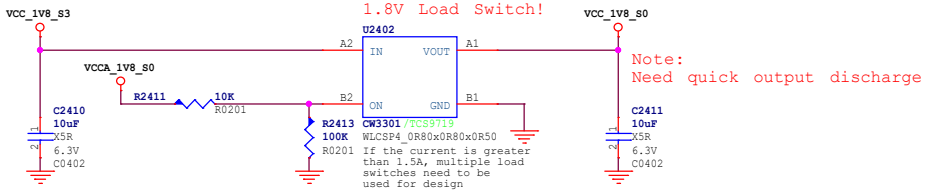
VCC_2V0_PLDO_S3



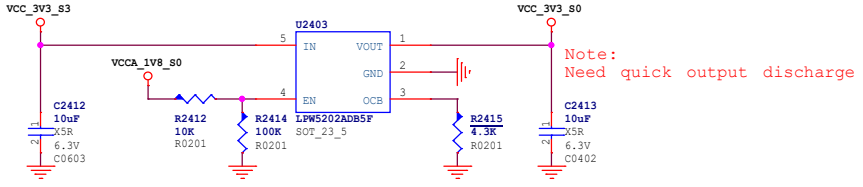
VCC_1V1_NLDO_S3



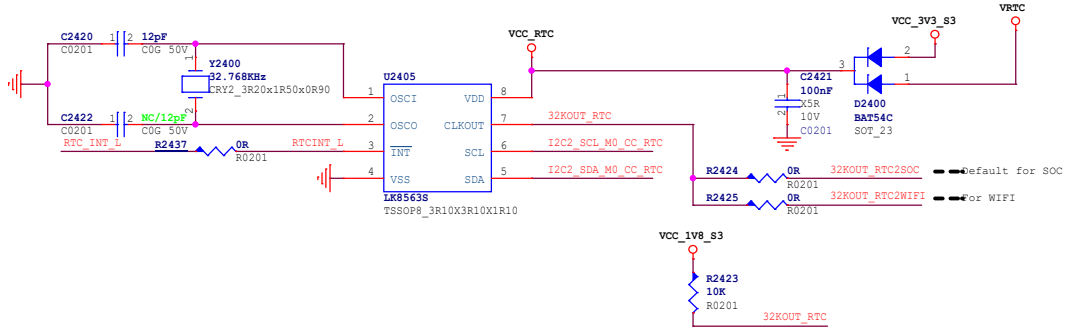
VCC_1V8_S0



VCC_3V3_S0



RTC



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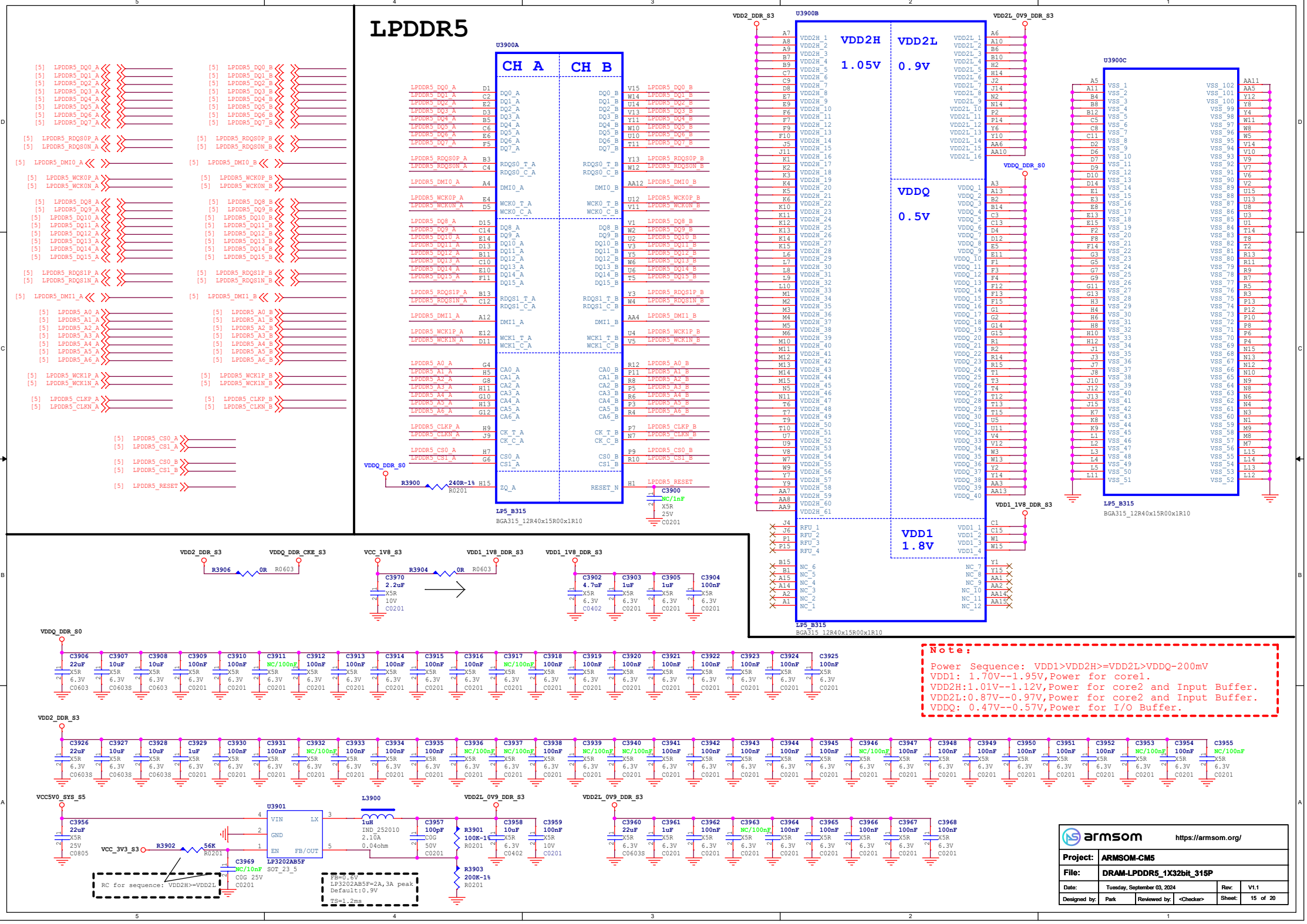
Project:	ARMSOM-CM5				
File:	Power-Ext Discrete/RTC IC				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 20

LPDDR5

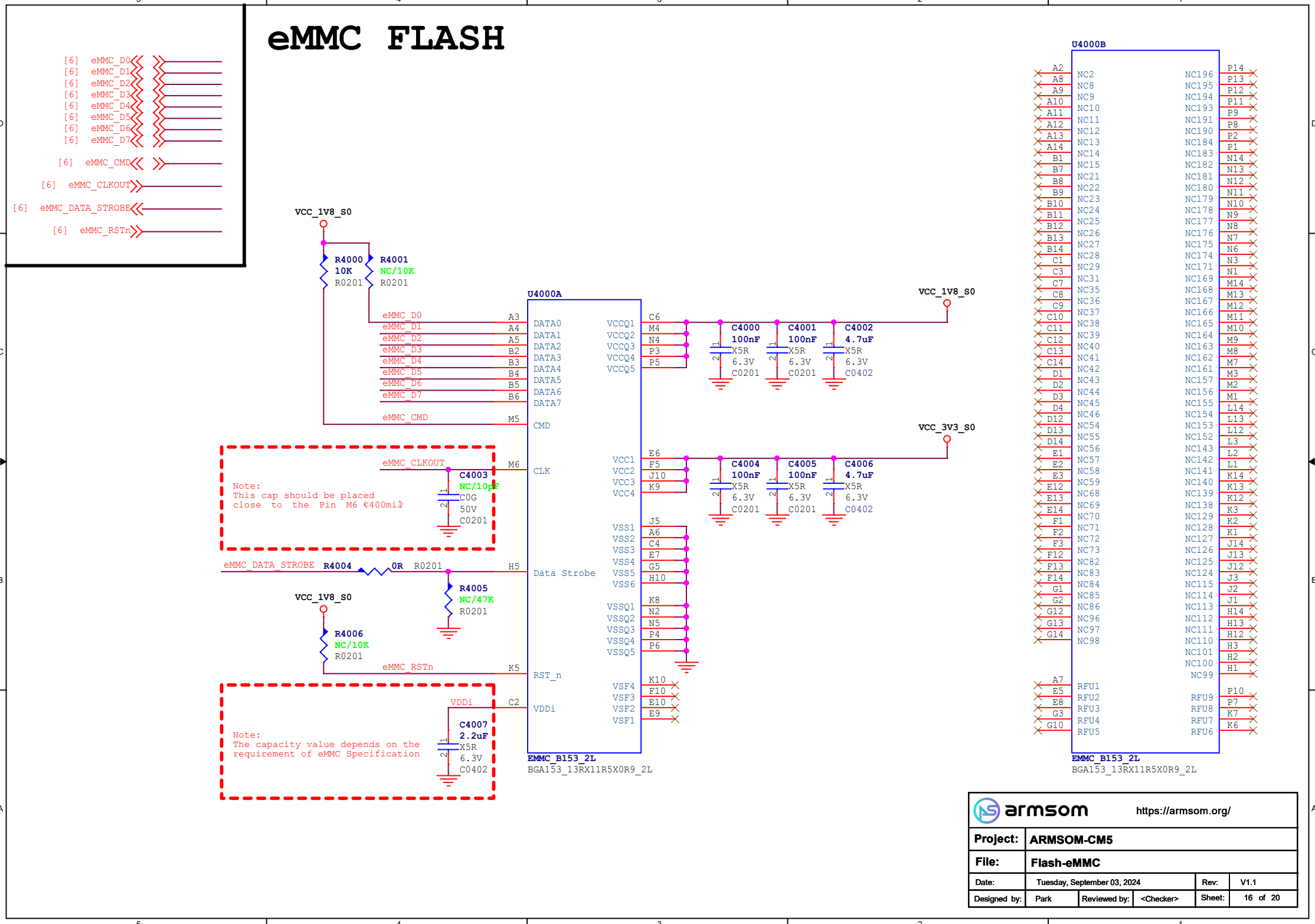


Note:

Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	DRAM-LPDDR5_1X32bit_315P				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 20

eMMC FLASH



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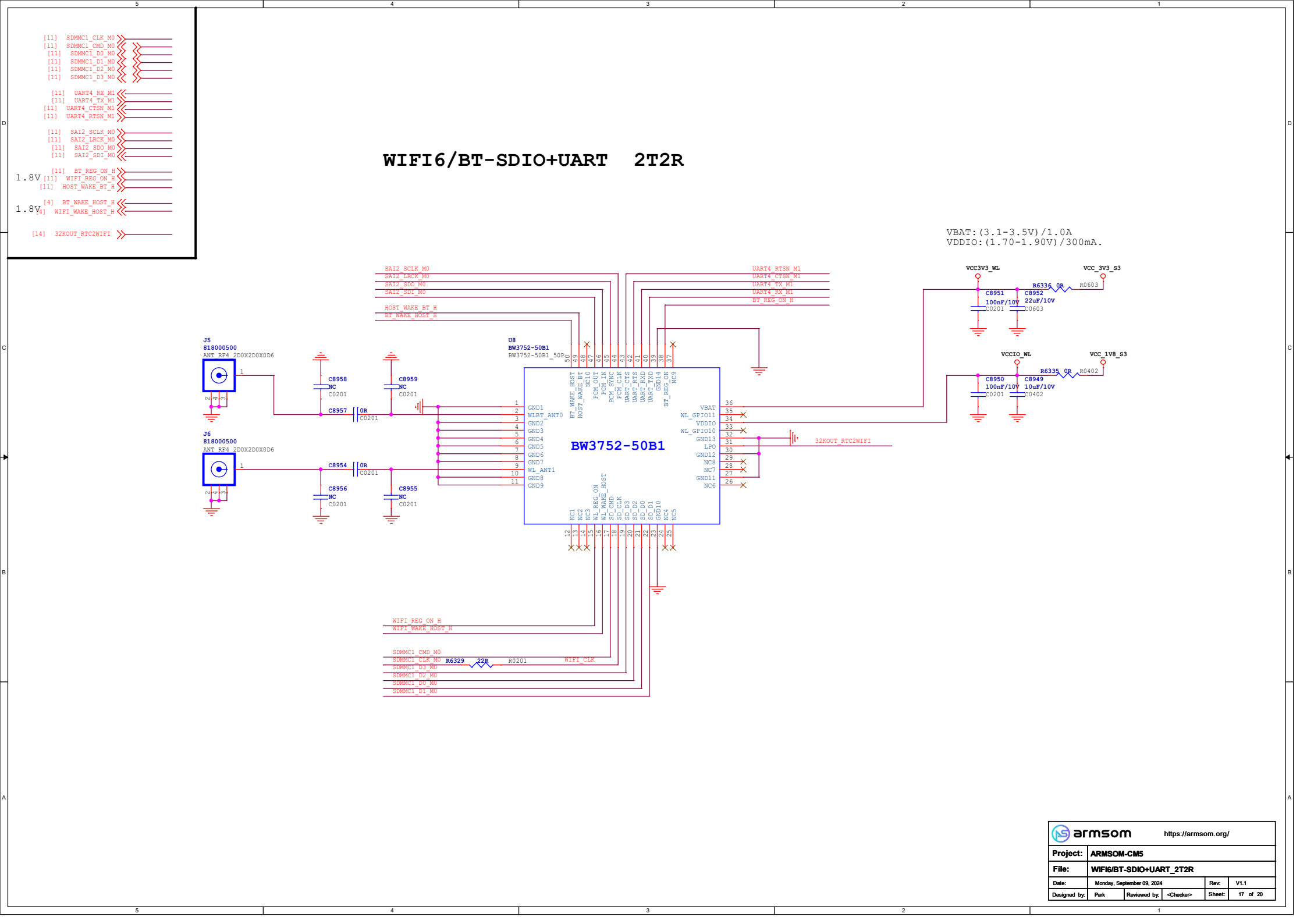
Project:	ARMSOM-CM5				
File:	Flash-eMMC				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 20

WIFI6/BT-SDIO+UART 2T2R



armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	WIFI6/BT-SDIO+UART_2T2R				
Date:	Monday, September 09, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	17 of 20

RGMII0_M0

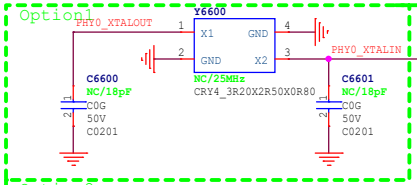
[12] GMAC0_TXD0_M0
[12] GMAC0_TXD1_M0
[12] GMAC0_TXD2_M0
[12] GMAC0_TXD3_M0
[12] GMAC0_TXCTL_M0
[12] GMAC0_TXCLK_M0

[12] GMAC0_RXD0_M0
[12] GMAC0_RXD1_M0
[12] GMAC0_RXD2_M0
[12] GMAC0_RXD3_M0
[12] GMAC0_RXCTL_M0
[12] GMAC0_RXCLK_M0

[12] ETH_CLK0_25M_OUT_M0

[12] GMAC0_MDC_M0
[12] GMAC0_MDIO_M0
[12] GMAC0_RSTn

Option1



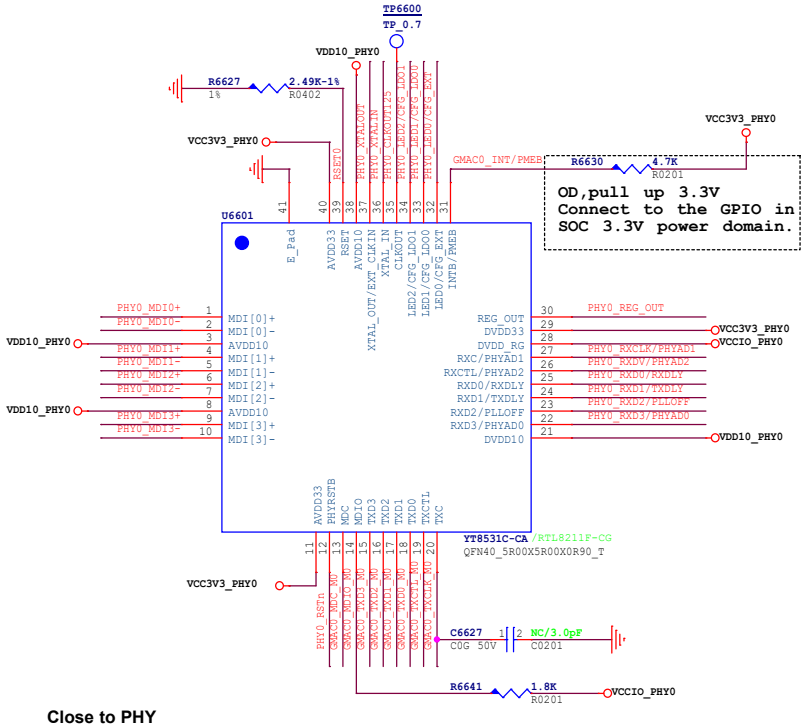
Option2

ETH_CLK0_25M_OUT_M0 R6613 0R R0201 PHY0_XTALOUT

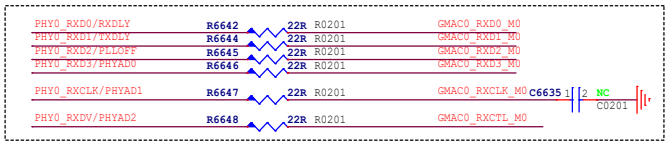
MAC -----> PHY

LAN Interface

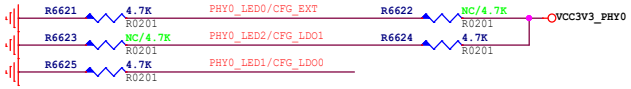
[19] PHY0_MDI3-
[19] PHY0_MDI3+
[19] PHY0_MDI2-
[19] PHY0_MDI2+
[19] PHY0_MDI1-
[19] PHY0_MDI1+
[19] PHY0_MDI0-
[19] PHY0_MDI0+
[19] LAN0_YLED-
[19] LAN0_GLED+



Close to PHY



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V (default)	1'b0	2'b10	String 510R to VCC3V3_PHY

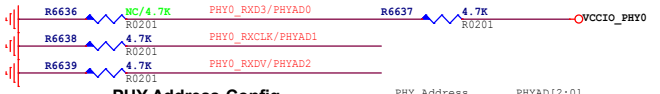


VCC_PHY0_IO Voltage Config

Pull-up to disable PLL @ ALDPS mode(Low power mode)

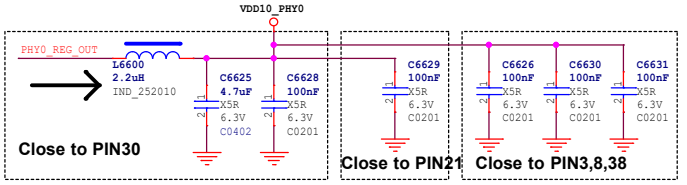
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

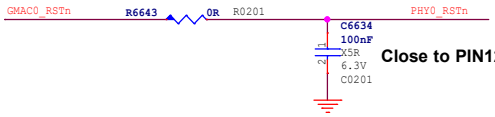


PHY Address Config

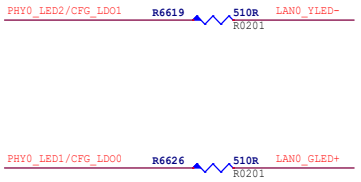
PHY Address	PHYAD[2:0]
1 (default)	3'b001

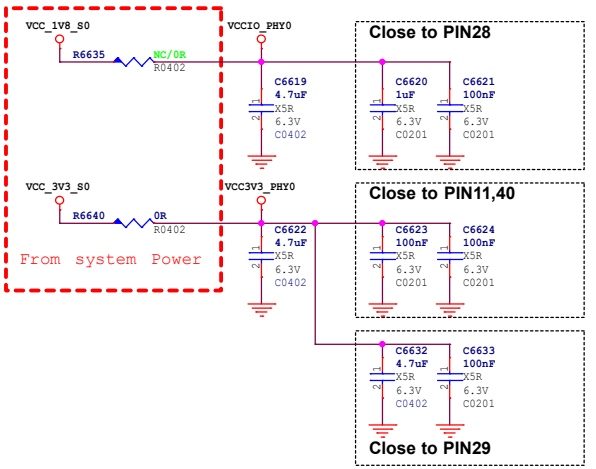


PHYRSTB is 3.3V IO



LAN0 LED





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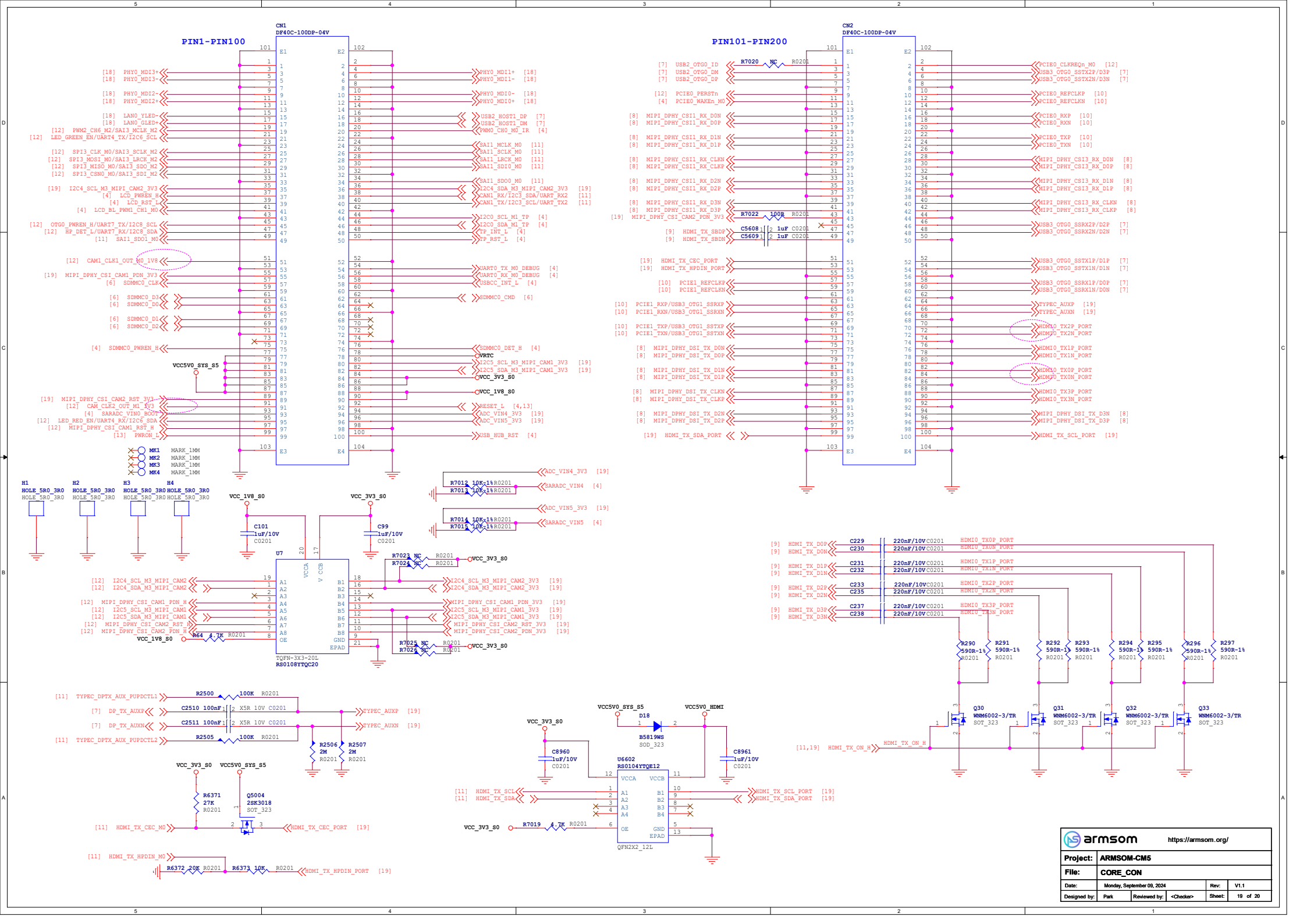
Project:	ARMSOM-CM5				
File:	Ethernet-GEPHY_RGMII0				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	18 of 20


PIN1-PIN100
CN1
DF40C-100DP-04V
PIN101-PIN200
CN2
DF40C-100DP-04V
armsom
https://armsom.org/
Project: ARMSOM-CM5
File: CORE_CON
Date: Monday, September 09, 2024
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 19 of 20

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2024-04-19	Park	1: First version;	
V1.0	2024-05-09	Park	1: del same caps and L3900/L6600 Footprints change to IND_252012 for layout; 2: del wifi module SDIO&I2S series resistors for layout;	
V1.0	2024-05-30	Park	1. C3926/C3927/C3928/C3960/C3907 pcbpackge change small for layout; 2. L2305/L2307 pcbpackge change small for layout;	
V1.1	2024-08-27	Park	1.Wifi module=BL-M8852BS2 change to BW3752-50B1; change CN1: pin51&pin91; 2. TF Card_DET: check Low change to Hight; 3. add hdmi circuit to mainboard;	

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	History				
Date:	Tuesday, September 03, 2024			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	20 of 20